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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/920,222
Filing Date: August 01, 2001
Appellant(s): DAVIES, ROBERT B.

Robert A. Parsons
For Appellant

EXAMINER'S ANSWER

This is in response to the supplemental appeal brief filed 5/21/04 and the appeal brief filed 12/22/03.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

Upon further review of the appellant's arguments, the statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1 thru 7, 28 thru 33, and 37 thru 51.

Claims 1, 2, 4 thru 7, 28 thru 33, 37, 41, 42, and 49 thru 51 are rejected.

Claims 45 thru 48 are allowed.

Claims 3, 38 thru 40, 43, and 44 are objected.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is substantially correct. The changes are as follows: Claims 45 thru 48 are allowed. Claims 3, 38 thru 40, 43, and 44 are objected.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief filed 12/22/03 is correct. There is no copy of the appealed claims in the supplemental appeal brief filed 5/21/04.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

3,881,244	Kendall	5-1975
4169000	Riseman	9-1979
JPO 06-120036	Matsuzaki	4-1994

(9) Grounds of Rejection

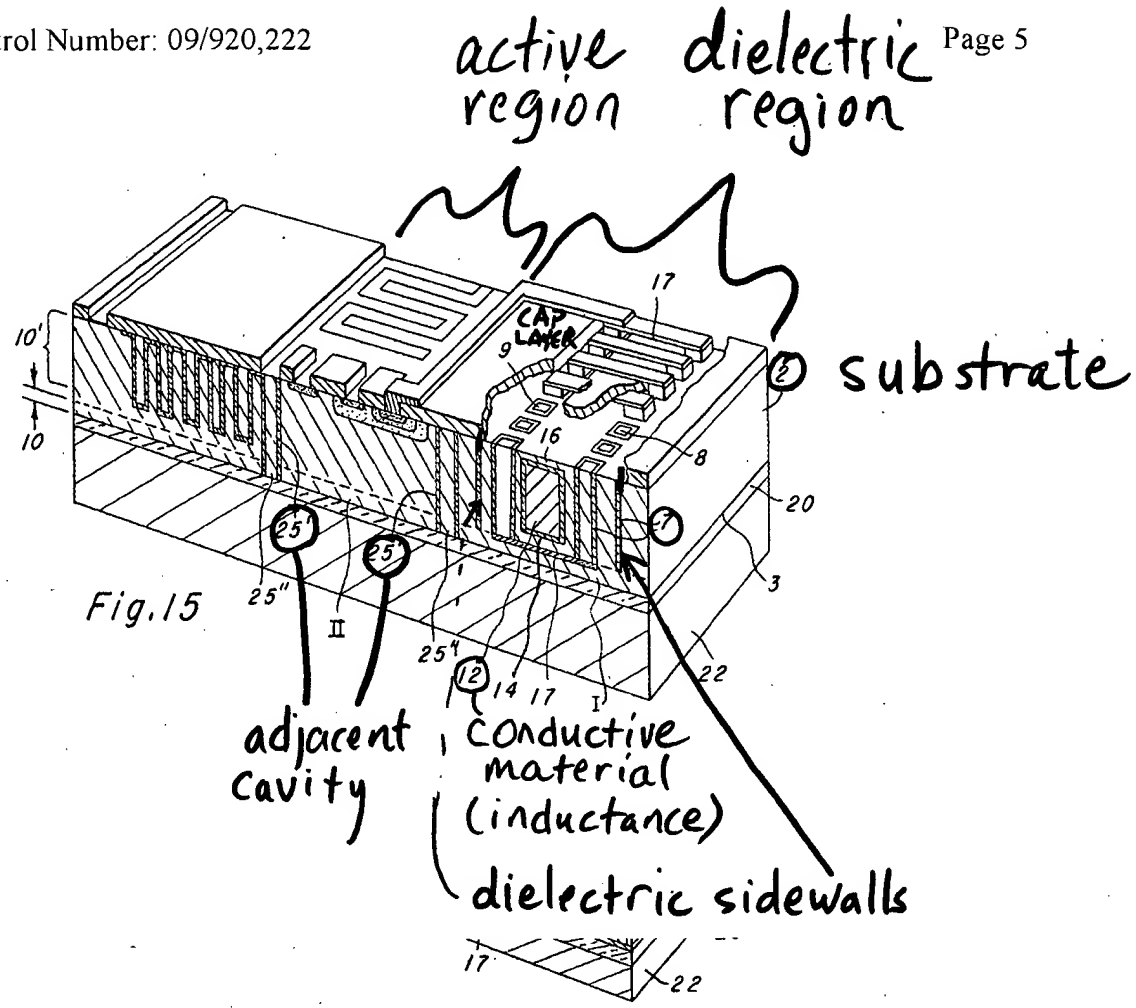
The following ground(s) of rejection are applicable to the appealed claims:

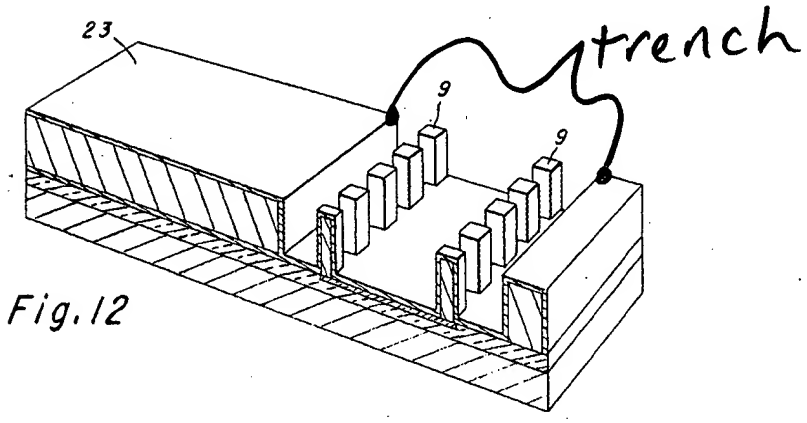
Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains: Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5 thru 7, 37, 42, 49, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall 3,881,244 in view of Riseman 4,169,000. Kendall discloses (see, for example, FIG. 15) an integrated circuit comprising a silicon substrate (low resistivity semiconductor substrate) 2, dielectric region, trench, oxide layer (dielectric sidewalls) 7, isolation region 25', and core material (conductive material) 12. The right side of the figure shows an inductance I.





Kendall does not disclose the isolation region 25' as a cavity. However, Riseman discloses (FIG. 7) an integrated circuit structure comprising a cavity 12. In column 4, lines 32-37, Riseman discloses the cavity as being air isolated and capable of absorbing changes in volume resulting

from processing steps. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the cavity of Riseman in Kendall's invention in order to absorb changes in volume resulting from processing steps.

In line 7 of claim 1, the limitation "electroplated" is a product-by-process limitation.

Regarding claim 2, see the cap layer as labeled in the figure above.

Regarding claim 5, see column 3, lines 23-25 wherein Kendall discloses the grooves as 15 mils (37.5 microns) deep.

Regarding claim 6, see FIG. 15 wherein Kendall discloses a silicon oxide layer (silicon based dielectric) 20.

Regarding claim 7, see FIG. 15 wherein Kendall discloses a transistor (active device) II.

Regarding claims 37, 42, and 49, Kendall discloses (see, for example, FIG. 15) an integrated circuit comprising a silicon substrate (low resistivity semiconductor substrate) 2, transistor (active region) II, dielectric region, trench, oxide layer (side-walls) 7, and metal core (high conductivity electroplated material) 12. The metal core is a portion of the inductor I.

Regarding claim 50, Kendall in view of Riseman does not disclose the low dielectric constant material having an effective dielectric constant of approximately 2.5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the low dielectric constant material having an effective dielectric

constant of approximately 2.5 because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the effective dielectric constant in order to provide adequate insulation in a semiconductor device.

3. Claims 4, 41 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kendall '244 in view of Riseman '000 as applied to claims 1, 2, 5-7, 37, 42, 49, and 50 above, and further in view of Matsuzaki 06-120036. Kendall in view of Riseman does not disclose the conductive material including copper. However, Matsuzaki discloses a semiconductor device comprising a trench 31 filled with copper. The copper serves as a conductive metal for an induction element such as an inductor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use copper in order to form an inductor with good inductive properties and increased current capacity.

4. Claims 28 thru 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki 06-120036 JPO in view of Kendall 3,881,244 in view of Riseman 4,169,000. Matsuzaki discloses (see, for example, figure 2) a semiconductor device comprising a substrate 61, insulating film (dielectric region) 32, and trench 31 filled with a high conductive material (first inductor and second inductor of electroplated conductive material). A first inductor is formed in the substrate 61 and a second inductor is formed in substrate 11. Matsuzaki does not disclose a cavity. However, Kendall discloses (see, for example, FIG. 15) a semiconductor device comprising an inductor I and an isolation region (cavity) 25. Kendall teaches (see, for example, column 7, lines 22-49) that this isolation region isolates different parts in an integrated

circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the isolation region (cavity) in order to isolate different parts of an integrated circuit so that no interference occurs between adjacent devices.

Matsuzaki in view of Kendall does not disclose the isolation region 25 as a cavity. However, Riseman discloses (FIG. 7) an integrated circuit structure comprising a cavity 12. In column 4, lines 32-37, Riseman discloses the cavity as being air isolated and capable of absorbing changes in volume resulting from processing steps. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the cavity of Riseman in order to absorb changes in volume resulting from processing steps.

Regarding claim 29, see figure 2 wherein Matsuzaki discloses an integrated circuit device (transistor) 20, which contains a switching transistor.

Regarding claim 30, see figure 2 wherein Matsuzaki discloses a portion of the first inductor formed below the top surface of substrate 61.

Regarding claims 31 and 32, see page 4 of translation wherein Matsuzaki discloses the coil as hundreds of micrometers.

Regarding claim 33, see figure 2 wherein Matsuzaki discloses an insulation film (dielectric layer) 62 between the first inductor and second inductor.

Product-by-Process Limitations

5. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In*

re Luck, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or *otherwise*. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

The limitation "electroplated" is a product-by-process limitation which adds no structural limitations to applicant's claimed product.

Allowable Subject Matter

6. Claims 45 thru 48 are allowed. The following is a statement of reasons for the indication of allowable subject matter: The references of record, either singularly or in combination, do not teach or suggest at least "an integrated circuit comprising: a sealed cavity at least partially defined by the substrate in the dielectric region and in communication with a lower portion of the high conductivity material in the trench" (claims 45-48).

7. Claims 3, 38 thru 40, 43, and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

(10) Response to Argument

These arguments mainly address the seven issues that are argued in the more recently filed Supplemental Appeal Brief filed 5/21/04. The Appeal Brief filed 12/22/03 addresses old grounds of rejection from a previous rejection (filed 7/30/03), however, many arguments in both appeal briefs are similar, and in instances where the Appeal Brief filed 12/22/03 contains arguments not reiterated in the Supplemental Appeal Brief, and whose relevance is still important in this case, those arguments will also be addressed.

Regarding Issue #1 on page 8, paragraph 1 of the Appeal Brief filed 12/22/03, the appellant argues the disclosure of Kendall discloses a solid state conductor and not an integrated circuit, this argument is not persuasive. Kendall clearly discloses (see, for example, Fig. 15) an integrated circuit wherein a passive device (inductor) is integrated with an active device (transistor). Furthermore, in column 1, lines 27-35, Kendall clearly states the object of the invention is to provide an integrated circuit having a semiconductor inductor therein. Such an object of the invention is the same as the appellant's invention wherein the appellant states on page 1 of the specification that the present invention relates in general to semiconductor devices and, more particularly, to integrated circuits formed with inductive components.

Before the Examiner continues to address the arguments in both the Appeal Brief and Supplemental Appeal, the Examiner would like to address the gist of the appellant's argument (see, for example, page 9, second paragraph of the Appeal Brief filed 12/22/03) that an inductance must include the vertical posts and interconnects to be called the term "inductance". According to Webster's Dictionary, an inductance is a property of an electric circuit by which an electromotive force is induced in it by a variation of current either in the circuit itself or in a

neighboring circuit. Clearly, a core of an inductor can have an inductance if surrounded by a coil structure. However, the term "inductance" does not inherently equate to the structure of a core and a coil structure together in one device. Inductance is a property and a core, when used in an inductor, will possess "inductance" by itself.

Regarding Issue #1 on page 4 of the Supplemental Appeal Brief filed 5/21/04, the appellant's argument is persuasive and the drawing objection withdrawn.

Regarding Issue #2 on page 4 of the Supplemental Appeal Brief filed 5/21/04, the appellant's argument is persuasive and the rejection withdrawn.

Regarding Issue #3 on page 7 of the Supplemental Appeal Brief filed 5/21/04, the appellant argues that taking the limitations as a whole, it is clear that nothing in the structure of Kendall even remotely suggests the claimed structure, the Examiner respectfully disagrees. It should first be noted that the appellant's invention is intended the same way as Kendall's invention, an inductance integrated with an active device. In any case, regarding how the Examiner interpreted Kendall's structure in view of the appellant's claimed structural limitations, see the figure from Kendall directly below.

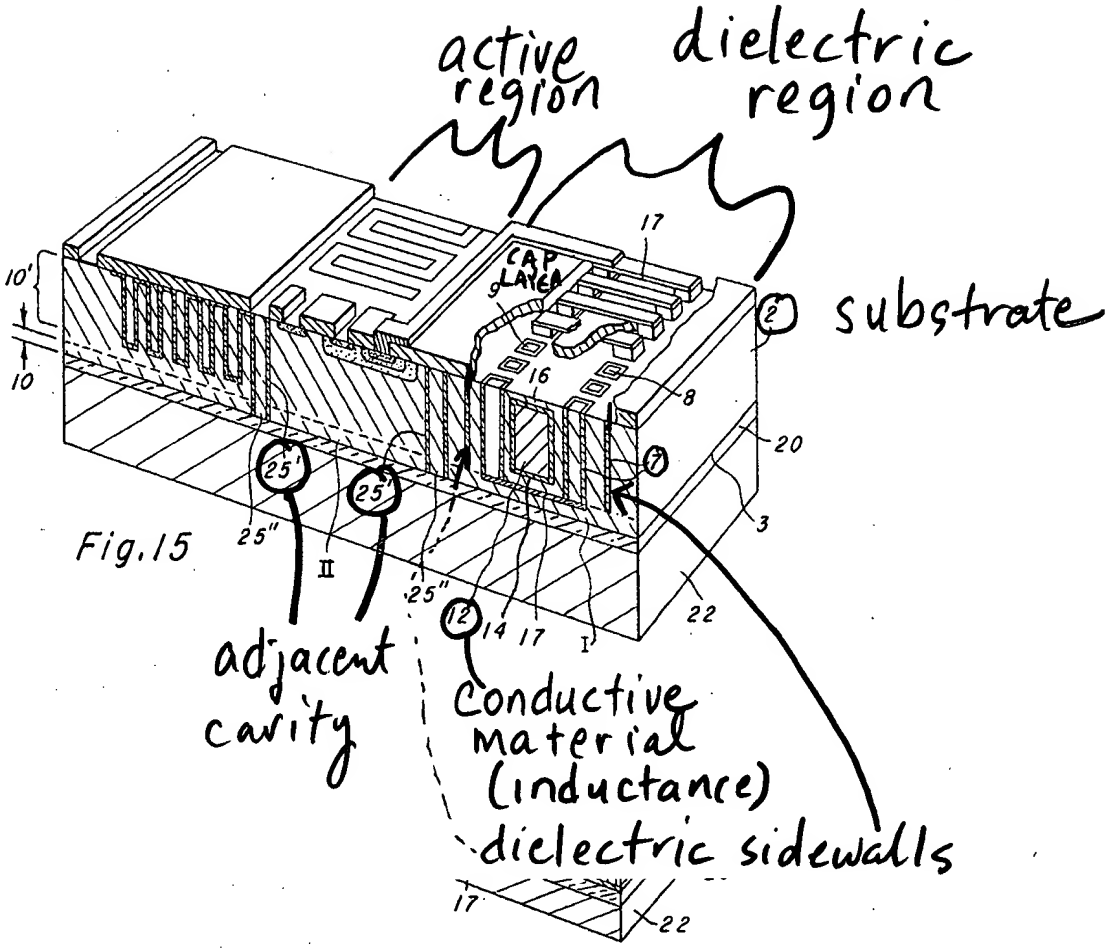


Fig. 15

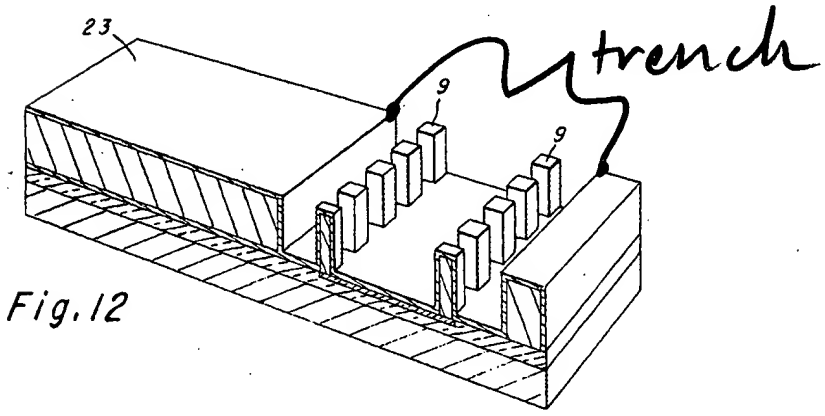


Fig. 12

In response to page 6, first paragraph of the Supplemental Appeal Brief, the Examiner confirms the entire right side as the "dielectric region" (the region that does not contain active devices). The "trench" is defined as the region between the studs 9 but also the region slightly outside of

studs 9. The oxide layer 7 is defined as the "dielectric sidewalls" but not the oxide layer 7 on the studs 9, but outside the studs 9 (as shown in the figure above). The "inductance" is core 12.

Regarding appellant's argument on page 7, second paragraph, that dielectric layer 7 on the sidewalls of studs 9 in Kendall are not and cannot be sidewalls of the trench, this argument is not persuasive. Looking at FIG. 15, the sidewalls of the trench is oxide layer 7 which is between stud 9 and isolation regions 25', NOT the oxide layer on the stud 9 as stated by appellant. This oxide layer is clearly the sidewalls of the trench. Regarding appellant's assertion in the same paragraph that core 12 of Kendall's inductance is not bounded by the sidewalls 9' of studs 9, this argument is not persuasive. The Examiner has defined the oxide layer 7 as the dielectric sidewalls, which clearly surround and bound the inductance 12. **In column 8, lines 66-67, Kendall discloses the core material 12 being chosen with a high permeability to provide a relative high inductance.** Clearly, from Kendall's disclosure, the core material has an inductance.

Regarding the applicant's argument on page 8, paragraph one, that the applicant's claimed inductance is an entire device and not a property, this argument is not persuasive. The first meaning of inductance according to Merriam Webster's Online Dictionary is a property of an electric circuit by which an electromotive force is induced in it by a variation of current either in the circuit itself or in a neighboring circuit. Clearly the core material 12 has an inductance and is bounded by oxide layer 7. It is not entirely clear why the appellant has neglected the first definition of inductance and reiterated the second definition which states that inductance is "a piece of equipment providing inductance in a circuit or other system". However, using the second definition, the core material would still be defined as an inductance since it is a piece of

equipment providing inductance in a circuit. It should further be noted that in claim 42 the appellant states a trench formed in the shape of an inductance and then states in independent claim 37 that high conductivity electroplated material in the trench defining a portion of a passive component. Such a shape of a trench (which has an inductance as stated in the appellant's claims) requires sides and a bottom.

Regarding appellant's argument on page 9, first paragraph, that Kendall's isolation regions 25 would not be adjacent the bottom of the inductance, this argument is not persuasive. First, the Examiner has interpreted the core 12 as the inductance. The studs 9 are not discussed in the rejection and were never interpreted by the Examiner as part of the inductance as stated in the appellant's claims. The Examiner has not interpreted helix as the inductance for one portion of the claim and core 12 as another portion as stated by the appellant. As stated in the rejection, the limitation "inductance" is interpreted as the core 12, not any other adjacent region (even though adjacent regions may **also** contain an inductance).

Regarding the applicant's argument on page 10, first paragraph, that interpreting the Kendall disclosure as one of ordinary skill in the art would interpret it, the compete inductance must include the helix formed by selectively interconnecting the upper and lower ends of studs 9 as well as core, this argument is not persuasive. The claims simply state an inductance that is bounded by sidewalls. Core 12 clearly has an inductance and it is bounded by sidewalls. Nowhere in the claims does the appellant state that the inductance must include a helix.

Regarding Issue #5 on page 13, paragraph 1, that the bottom of the inductor will not be positioned adjacent the cavity, this argument is not persuasive. The Webster's Dictionary defines the word "adjacent" to be "not distant". Clearly by adding the Kendall's isolation

region, it is "adjacent" to the first inductor. The appellant admits that the side of the inductor will be closest to the cavity and having it "closest to the cavity" would make it adjacent.

Regarding Issue #6 on page 14 of the Supplemental Appeal Brief filed 5/21/04, the appellant's argument is persuasive and the rejection withdrawn.

Regarding Issue #7 on page 16, paragraph 1 that appellant disagrees with the Examiner's assertion that the claimed limitation "electroplated conductive material" is a process limitation that does not add any structural limitations, this argument is not persuasive. The appellant states other regions that may have an inductance, i.e. interconnect, studs; however, these regions were not interpreted as the inductance as disclosed in the appellant's claims. The appellant further argues that different conductive material cannot be electroplated. However, the core 12 is metallic (see, for example, column 4, line 28 of Kendall) which is a material that can clearly be electroplated.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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SUPERVISORY PATENT EXAMINER

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February 7, 2005

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